Physical Modeling and Optimization of a GaN HEMT design with a Field Plate Structure for High Frequency Application

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Abstract— **In this paper, physical modeling of a GaN HEMT with a field plate structure is proposed, with the objective of providing the connection between the physical design parameters of the device (geometry, Al mole fraction, type of the field plate, etc) and on-resistance together with parasitic capacitances of the device. In this way, it is possible to optimize the design of a switching device for a particular application, which in our case is a high frequency DC DC converter for Envelope Tracking and Envelope Elimination and Restoration techniques. In this work, extrinsic models for output characteristics together with input, output and reverse capacitance of a depletion mode GaN HEMT with a field plate structure were obtained. The obtained physical model was implemented in a Simplorer simulation model of a high frequency buck converter and verified by the prototype that employed modeled GaN HEMT, operating at 7, 15 and 20MHz of switching frequency. Comparing to the measured efficiency curves, simulation results showed good agreement, especially in the low power range at high switching frequency, which are the operating conditions in our application.**

I. INTRODUCTION

Nowadays, new technological solution for switching devices based on Gallium Nitride is the most promising option for high frequency applications [1]. Comparing to standard Si MOSFETs, aforementioned GaN High Electron Mobility Transistors (HEMTs) provide several times better Figure Of Merit, because of their wider bandgap, higher critical electric field and saturation velocity [2, 3]. Additional application of the so-called field plate structure, provided even higher breakdown voltages and lower gate leakage currents [4]. On the other hand, one of the major drawbacks of these devices, known as dynamic on – resistance or current collapse phenomena, has been the topic of many research activities in the past couple of years and significant technological improvement has been obtained in this direction as well [5, 6].

Speaking of high frequency power electronics applications such as Envelope Amplifier in Envelope Tracking and Envelope Elimination and Restoration techniques, the main challenge designers are facing is the efficiency increase of the signal transmission, simultaneously with the bandwidth [7-12]. Envelope Amplifier that was considered in our previous work was a high frequency buck converter with GaN HEMTs used instead of Si MOSFETs [13]. In order to improve the design of existing GaN devices for this particular application, it is necessary to obtain the physical model that provides the relations between the design parameters such as geometry of the device, type of the field plate, number of paralleled fingers etc. with switching on-resistance and parasitic capacitances. Physical model is a necessary connection between the device itself and its application. Using the electrical model, we are providing the relation between the physical design and the circuit (Fig. 1). In this way, it is possible to close the "loop" presented in Fig. 1, and obtain the optimum design of a switching device by minimization of the power losses in a particular application. This was the main motivation for the work presented in this paper.

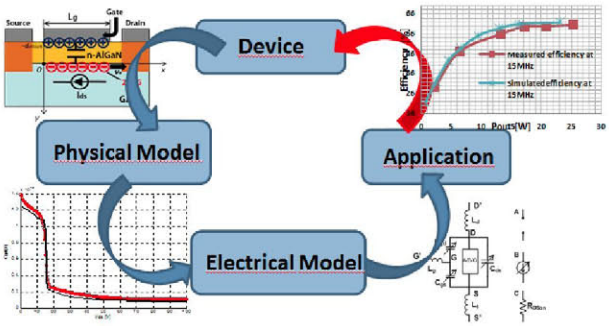

Figure 1. The block scheme of device design optimization

II. 2DEG SHEET DENSITY CONTROL BY SCHOTTKY GATE

The starting point of the physical model certainly is the dependence of the 2DEG, formed in the quantum well at the AlGaN/GaN heterojunction, on the applied gate voltage (Fig. 2). When a Schottky gate is in contact with AlGaN, two depletion layers are formed within AlGaN: the surface Schottky depletion layer and the AlGAN/GaN heterojuction depletion layer. For optimum performance, the layer thicknesses are designed in a way that these two depletion layers overlap which prevents any current conduction through AlGaN part. By applying Poissons equation to AlGaN and GaN layer, together with Gauss law for charge conservation at the heterojunction, we obtain the following equation [14]

$$n_{2DEG} = \frac{\varepsilon_a(m)}{q(d_d+d_{sp})}\left(V_g - V_{th}(m) - \frac{E_F}{q}\right) \quad (1)$$

where n_{2DEG} is the 2DEG sheet density, E_F is the Fermi energy (in eV), q is the electron charge, m is the Al mole fraction in $Al_mGa_{(1-m)}N$, $\varepsilon_a(m)$ is the permittivity of $Al_mGa_{(1-m)}N$, d_d and d_{sp} are the thickness of doped and spacer layer in AlGaN, respectively, V_g is the applied gate voltage and V_{th} is the threshold voltage given by the following equation

$$V_{th}(m) = \phi_S(m) - \Delta E_C(m) - \frac{qN_D d_d^2}{2\varepsilon_a(m)} - \frac{\sigma_{PZ}(m)}{\varepsilon_a(m)}(d_d + d_{sp}) \quad (2)$$

In the previous equation, $\phi_S(m)$ is the height of the Schottky barrier at gate- AlGaN heterojunction (1.165V), $\Delta E_C(m)$ is the conduction band discontinuity at the AlGaN/GaN interface (the height of the quantum well) equal to 0.343V while $\sigma_{PZ}(m)$is the polarization-induced charge density of 0.0105C/m^2 and is calculated using [15]. For analyzed GaN HEMT, Eq. (2) gives a threshold of -2.0899V which is in good agreement with the measured value of -2V.

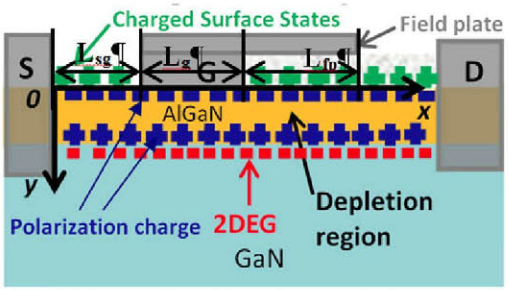

Figure 2. Cross section of a GaN HEMT with a field plate

In order to obtain the relation between the 2DEG and Fermi energy, it is necessary to use Fermi-Dirac statistics. If we assume triangular approximation of the quantum well (where 2DEG is being formed), with only the first two subbands E_0 and E_1 possibly occupied, the 2DEG can be presented as [14]

$$n_{2DEG} = Dk_BT\left[\ln\left(1+e^{\frac{(E_F-E_0)}{k_BT}}\right)+\ln(1+e^{\frac{(E_F-E_1)}{k_BT}})\right] \quad (3)$$

In Eq. (3), k_B is the Boltzmann's constant, $D = 4\pi m_{le}^*/h^2$ is the density of states for each subband, T is the temperature, m_{le}^* is the longitudinal effective mass of electron (= $0.22m_e$ with m_e as the electron mass), and h is the Planck's constant. The aforementioned subbands E_0 and E_1 are related to the 2DEG density as: $E_0=\lambda_0 n_{2DEG}^{2/3}$, $E_1=\lambda_1 n_{2DEG}^{2/3}$ in (eV), with $\lambda_0=2.123*10^{-12}$ and $\lambda_1=3.734*10^{-12}$ [14]. In order to obtain the Fermi level dependence on the applied gate voltage, model from [16] was used to approximate (3) for different relative positions of E_f, E_0 and E_1. Finally, using that model together with (1) and (2), the 2DEG sheet density dependence is obtained and presented in Fig. 3. In this case, it is considered that applied drain-to-source voltage is equal to zero voltage. Using the approach from [16], it has been established that for V_g equal to 0.71V, Fermi level reaches the value of the quantum well height, ΔE_C=0.343V, which means that 2DEG in the well is starting to saturate and we are losing the 2DEG control by the gate voltage. The parameters of analyzed GaN HEMT are given in the Table 1.

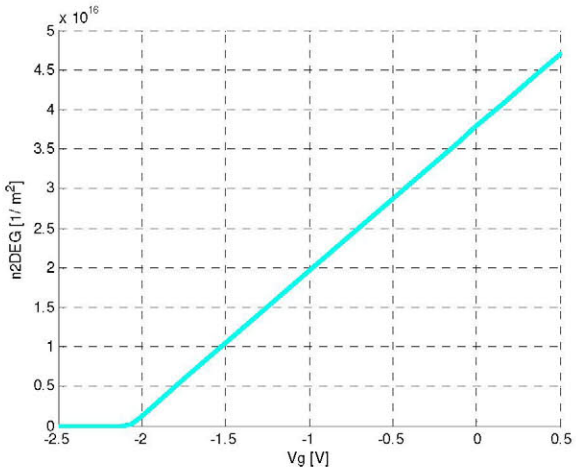

Figure 3. 2DEG sheet density dependence on the applied gate voltage

TABLE I. PARAMETERS OF THE ANALYZED GAN HEMT

W_g [mm]	L_g [um]	L_{sg} [um]	L_{fp} [um]	t_{ox} [nm]	d_d [nm]	d_{sp} [nm]	m [%]	N_d [1/m^3]
120	2	2	1.5	80	20	3	25	10^22

III. EXTRINSIC MODEL FOR THE DRAIN CURRENT DEPENDENCE ON GATE-SOURCE AND DRAIN-SOURCE VOLTAGES

Since the gate control of the 2DEG sheet density has been modeled and obtained, it is possible to obtain extrinsic model for output characteristics, I_d (V_{ds}, V_{gs}), of a HEMT. The drain current in the channel can be presented by the following equation [14]:

$$I_d = q\,W_g v_{DRIFT}(x) n_{2DEG}(x) \quad (4)$$

where W_g is the gate width and $v_{DRIFT}(x)$ is the electron velocity given by

$$v_{DRIFT}(x) = \frac{\mu_0}{1+\frac{E(x)}{E_C}} E(x) \quad for\ E(x) < E_C \qquad (5a)$$

$$v_{DRIFT} = v_{SAT} \quad for\ E(x) > E_C \qquad (5b)$$

In the previous equations, electric field $E(x)=dV_C(x)/dx$ is the lateral electric field at the point x in the channel, $V_C(x)$ is the potential in the channel, μ_0 is the low field mobility of 2DEG (equal to 1000 cm^2/Vs), E_C is the critical electric field and v_{SAT} is the saturation velocity equal to $3.775*10^5$ m/s.

In order to obtain extrinsic model for the linear region of output characteristics we solve (4) under the boundary conditions: $V_c(x=L_{sg})=I_d$ $(R_{s\_cm}+R_{s\_drift})$ and $V_c(x=L_{sg}+L_g)=V_{ds}-I_d$ $(R_{d\_cm}+R_{d\_drift})$. In the previous calculation, R_{s_cm} and R_{d_cm} are source and drain resistances due to the metallization and contacts, (around 25mΩ each), while R_{d_drift} and R_{s_drift} are drain and source drift resistances.

The first approximation of source and drain drift resistance, was made by taking the voltage drop from the simulation of the channel potential distribution (Fig. 4) and dividing it by the measured drain current in that point. The values obtained in this way were equal to 63 and 31.5 mΩ for drain and source drift resistance, respectively.

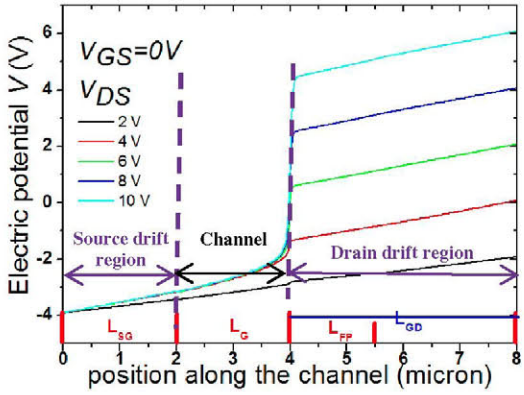

Figure 4. Simulation of the electric potential along the channel

These resistances can be modeled in the following manner:

$$R_{D\_DRIFT} = \frac{L_{gd}}{q\mu_0 W_g n_{S0}}; \quad R_{S\_DRIFT} = \frac{L_{gs}}{q\mu_0 W_g n_{S0}} \qquad (6a, b)$$

In (6a, b), n_{S0} corresponds to the value of the 2DEG sheet density in the areas between the source contact and the channel and the drain contact and the channel. This value can be obtained from n_{2DEG} (V_g) for gate voltage equal to zero. In the case of analyzed GaN HEMT, with parameters from Table 1 and previously obtained sheet dependence on the V_g, modeled drain and source drift resistances are equal to 54.8 and 27.4 mΩ, respectively. The modeled values are different from previously obtained values from the simulation for around 13%, which corresponds to the error of 8 mΩ.

The saturation part of output characteristics, has been modeled by taking into account the channel length modulation [17]. The obtained model for extrinsic I_d (V_{gs}, V_{ds}) together with measured curves, is presented in Fig. 5. It can be seen that in the linear part (which is the area of interest for the switching application), there is a very good agreement between the model and experimentally obtained values. On the other hand, the highest error of the model, equal to 32% has been obtained for V_{gs}=-1.5V (just above the threshold), deeply in the saturation area. This error and higher slope of the measured output characteristics (comparing to the modeled ones) are, most likely, caused by additional effect of the field plate structure on the channel length modulation, that was not considered in the model.

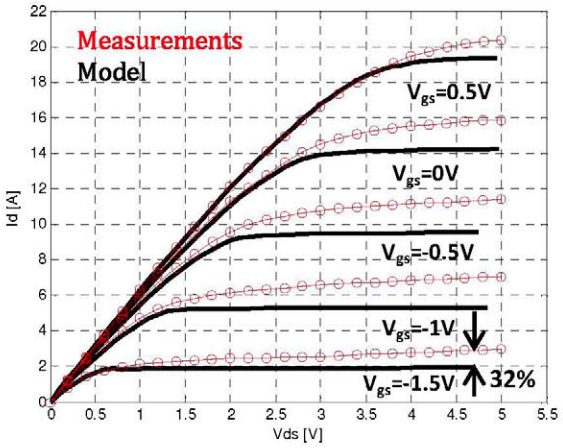

Figure 5. Extrinsic I_d (V_{ds}, V_{gs}) characteristics of the HEMT: measured -red and modeled –black

IV. EXTRINSIC MODEL FOR PARASITIC CAPACITANCES

From the point of view of switching applications, values of parasitic capacitances and their nonlinear behavior is crucial in the process of device design optimization. In order to obtain the model that can be implemented in the simulation program such as PSpice or Simplorer, it necessary to obtain the dependence of input, output and reverse capacitance on drain-to-source voltage, when the transistor is turned off.

A. Millers capacitance modeling in the subthreshold regime

In order to find the origin of Millers capacitance (C_{gd}), we will observe the simulation of the 2DEG distribution in the channel, for V_{gs}=-3V and V_{ds} being changed from 10 to 60V (Fig. 6). It can be seen, that the main part of 2DEG leftover under the field plate is being depleted for V_{ds} lower than 20V, caused by the electric field component perpendicular to the channel, E_y. On the other hand, lateral component of the electric field will provide additional extension of this depletion area in the whole range of V_{ds}. The simulation of the lateral component of the electric field, E_x, is presented in Fig. 7.

In order to physically model 2DEG depletion process under E_y component, the following methodology was proposed.

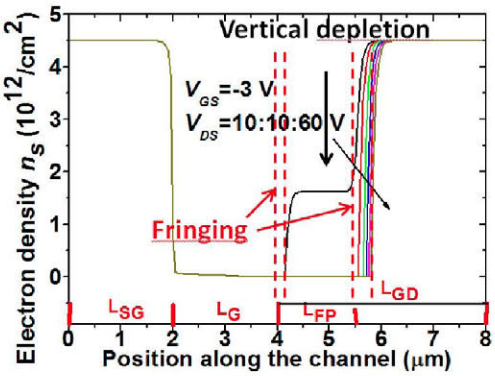

Figure 6. Simulation of 2DEG depletion in the channel, with increase in V_{ds} from 10V (black) up to 60V (green), with a 10V step

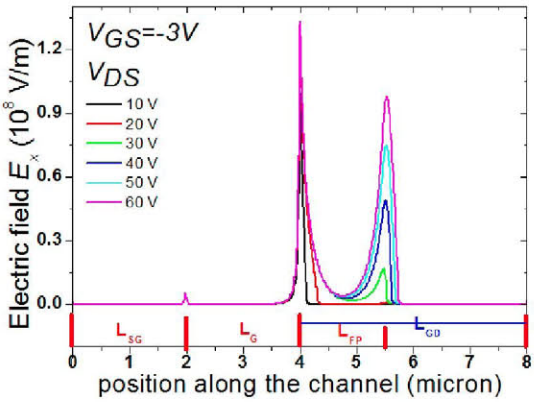

Figure 7. Simulation of lateral electric field in the channel

Since V_{gs} is constant and V_{ds} is being changed, the metal-insulator-semiconductor structure has been analyzed and its 2DEG sheet density dependence on the V_{gd} was obtained. The closed form solution for this dependence is:

$$n_{2DEG_{FP}}(V_{gd}) = \frac{\sigma_{PZ}}{q} - \frac{\varepsilon_a}{q}\frac{-V_{gd}+\phi_b-\Delta E_C+\frac{qN_d\left((t_{ox}-d_d)^2-d_{sp}^2\right)}{2\varepsilon_a}+qt_{ox}N_d\frac{(t_{ox}-d_d)}{\varepsilon_{ox}}}{t_{ox}\left(1+\frac{\varepsilon_a}{\varepsilon_{ox}}\right)-(d_d+d_{sp})} \quad (7)$$

In (7), ϕ_b is the metal –insulator barrier height (equal to 2.2V), t_{OX} and ε_{OX} are the thickness and permittivity of the field plate. From (7), using $V_{gd}=V_{gs}-V_{ds}$ and $C_{gd}(V_{ds})=q\,L_{FP}W_g\,dn_{DEGFP}/dV_{ds}$, we obtain the expression for the part of C_{gd} caused by the E_y, C_{gdy}:

$$C_{gdy}(V_{ds}) = L_{FP}W_g\frac{\varepsilon_a}{\left(t_{ox}\left(1+\frac{\varepsilon_a}{\varepsilon_{ox}}\right)-(d_d+d_{sp})\right)} \quad (8)$$

For V_{ds}>16.5V, $C_{gdy}(V_{ds})$=0. In the case of analyzed HEMT, this value is equal to 96.3pF.

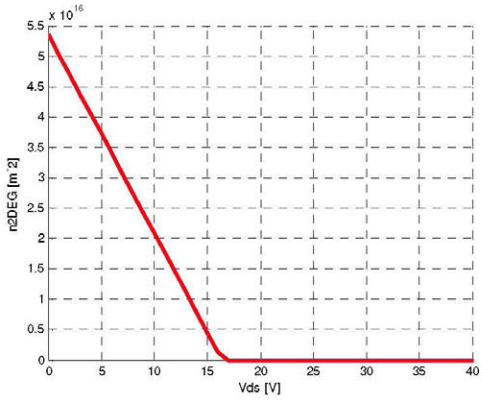

Figure 8. Modeled 2DEG depletion under the field plate

In order to model fringing of the depletion area in x-direction, conformal mapping technique has been used [18]. In that way, depletion area extension dependence on the applied V_{ds} has been obtained. In the range of drain voltages lower than 16.5V, this capacitance is added to the C_{gdy} to obtain total Millers capacitance, while for higher V_{ds}, this fringing part represents the total C_{gd}. The comparison between the obtained model and the measurements is presented in Fig.9. It can be seen that the knee voltage has been modeled precisely and that the highest error of 22% is obtained in the fringing area, where the capacitance values have the order of pF.

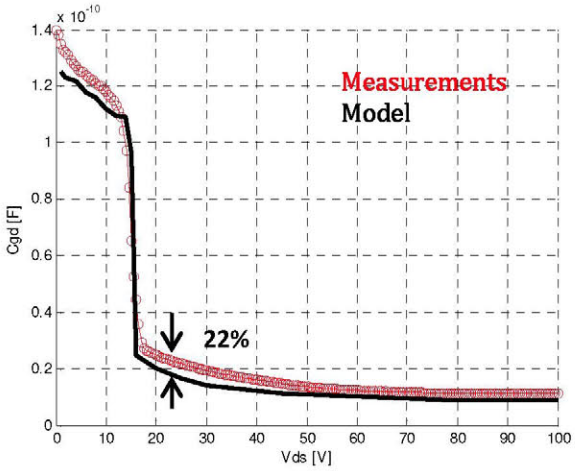

Figure 9. Modeled C_{gd} (black) versus measurements (red)

B. *Input and output capacitance modeling in the subthreshold regime*

Speaking of output capacitance, $C_{oss}=C_{gd}+C_{ds}$, it was necessary to determine the capacitance between drain and source terminal of the device. This capacitance mainly depends on the geometry of the device and how the metal layers are placed. In the case of analyzed transistor, the main part of this capacitance is caused by the fringing

between drain and source electrodes through GaN layer. For the given geometry, C_{ds} is equal to 40pF.

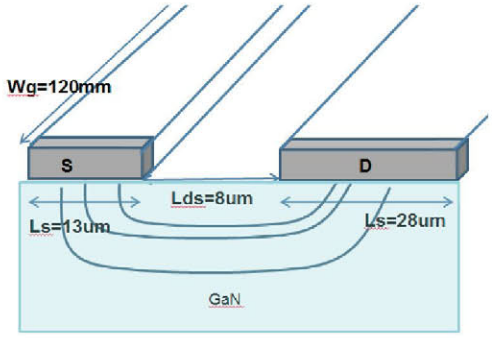

Figure 10. Drain-to-source capacitance caused by the fringing between drain and source electrodes

Gate to source capacitance also has the origin in the fringing between gate and source electrodes through AlGaN layer. Using the model from [19], it has been established that the highest portions of this capacitance are contained in the fringing between the sidewall of source electrode and the bottom of the gate as well as in the extension of the source electrode through undepleted 2DEG in the source drift area and the bottom of the gate electrode (Fig 11). In total, this part of C_{gs} has the value of 246pF.

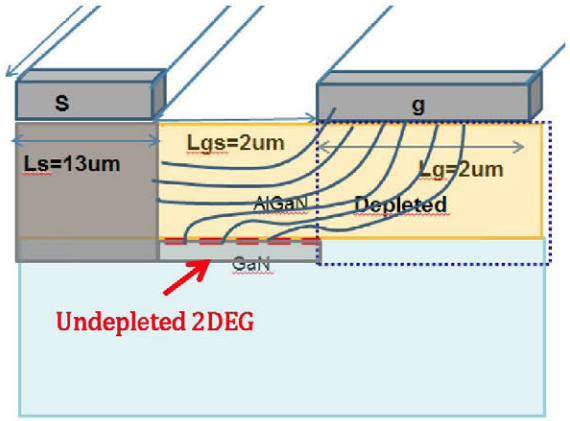

Figure 11. The part of C_{gs} caused by the fringing between the electrodes

In order to complete the capacitance modeling of a GaN HEMT with the field plate structure, it was necessary to analyze the multifinger configuration of the device and find all the additional sources of the capacitace. For this kind of observation, the Nomarski microscope was used to establish the surface distances between the fingers (Fig. 12), while the SEM (Scanning Electron Microscope) was used for observation of the air-bridges that connect source and drain fingers and their thicknesses (Fig. 13 and 14). Using the data about the surface geometry as well as the cross section geometry, it was possible to calculate the additional parasitic capacitances in the device, caused by the multifinger structure.

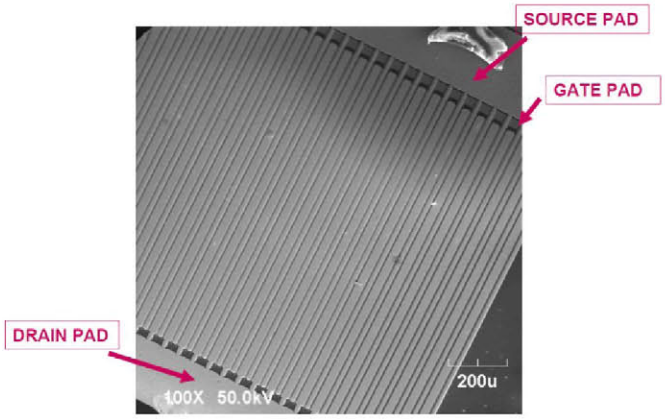

Figure 12. The top view of the multifinger configuration of the device

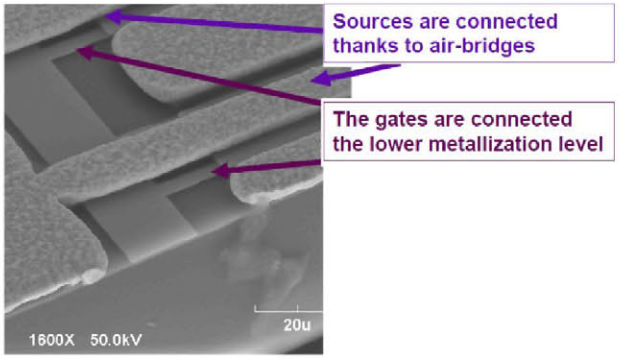

Figure 13. Connection of the fingers through air- bridges (source and drain) and lower metalization level (gate)

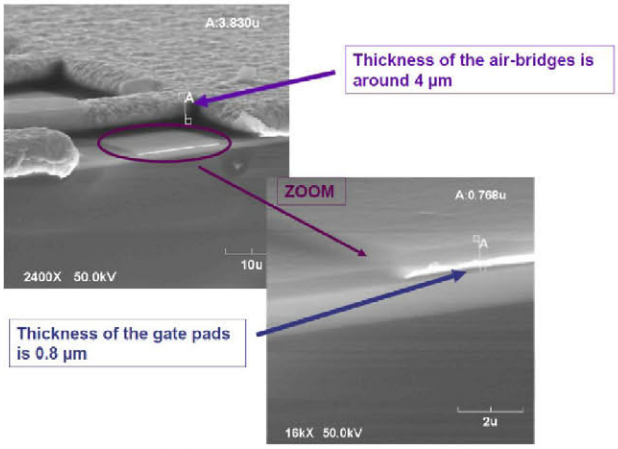

Figure 14. Cross section and relevant thicknesses

All of these capacitances were very small (the order of fF), except the one which was caused by the fringing through AlGaN and GaN layers between the surfaces that connect all gate and source fingers and are placed quite close (Fig. 15).

This capacitance is equal to 97 pF in the case of analyzed HEMT and presents quite a big portion of total C_{gs}.
The complete capacitance model versus measured curves is presented in Fig. 16. It can be seen that the highest error of the presented model, of approximately 40%, was found for high values of drain-to-source voltage in the output capacitance of the device. In this area, C_{gd} consist of the fringing part only, while C_{ds} has the constant value of 40pF as it was previously established. This error is, however, quite small if we observe absolute units of the modeled and measured capacitance and won't have significant influence on the power losses in our high frequency buck converter (as it will be shown in the next section).

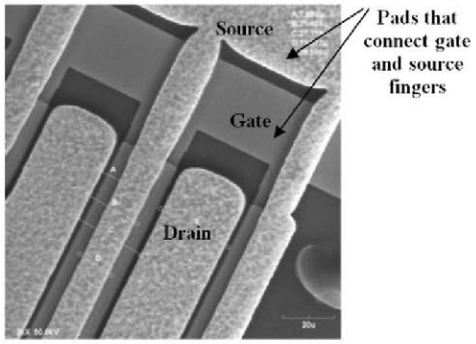

Figure 15. Fringing between gate and source finger-connecting pads

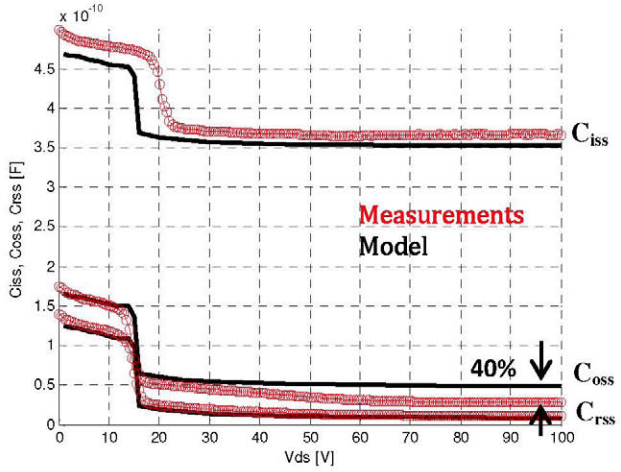

Figure 16. Complete model versus measurements for C_{iss}, C_{oss} and C_{rs}

C. *Input capacitance dependence on the gate voltage*

Input capacitance dependence on the gate voltage has been previously analyzed and modeled in [20-22]. This capacitance is dominantly influenced by the change in the 2DEG sheet density when HEMT is being turned on and has a big step around threshold. For the values lower than the threshold, this capacitance has previously obtained value in the subthreshold regime for V_{ds}=0, $C_{ISS,sub}$. The analyzed dependence can be presented by the following equation

$$C_{ISS}(V_g) = qW_gL_g\frac{dn_{2DEG}}{dV_g} + C_{ISS,sub} \quad (9)$$

The comparison between the measurements and the obtained model is presented in Fig. 17. It can be seen that the knee voltage i.e. the threshold was modeled precisely, while there is an error of approximately 6% in the subthreshold area. From this information, we can obtain the gate charge dependence on the gate voltage.

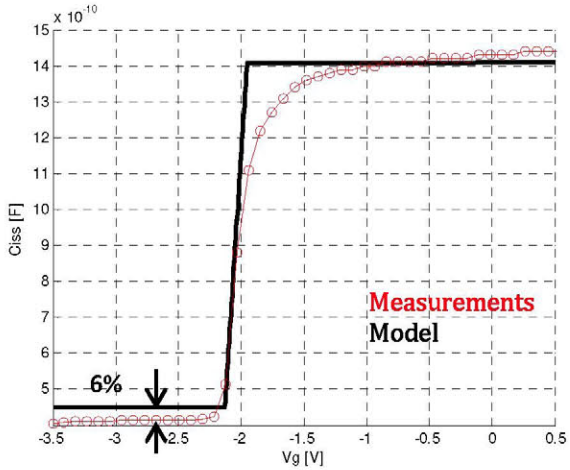

Figure 17. Extrinsic C_{iss} (V_{gs}): measured -red and modeled –black

V. IMPLEMENTATION OF THE OBTAINED PHYSICAL MODEL INTO THE SIMULATION MODEL AND COMPARISON WITH THE MEASURED EFFICIENCY CURVES

The target application for the modeled GaN HEMT is a high frequency DC/DC converter used as the dynamic power supply in ET and EER techniques (Fig. 18).

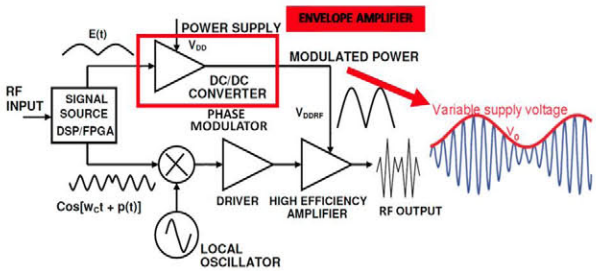

Figure 18. Block Scheme of Kahn (EER) Technique Transmitter

In order to verify the proposed physical model, the prototype of the HF buck converter was built, using the GaN device that was analyzed in this work. The diode that was used was low drop Schottky diode, STPS20LCT from ST microelectronics. The driving signal for depletion mode GaN HEMT was generated using Spartan 3 FPGA board, commercially available ISO721 isolation chip and EL7155 driver, with the adjustment of the gate-signal levels to -5V

(off-state) and 0V (on-state). The converter operated in open loop.

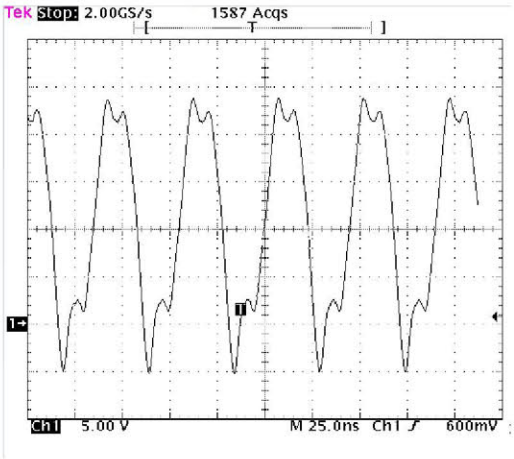

Figure 19. Input of the LC filter of the buck converter prototype at 25MHz

Efficiency measurements were done at 7, 15 and 20MHz of the switching frequency, changing the duty cycle in order to provide different output power levels (Fig. 20). The load resistance was set to 6Ω.

As it was previously explained, the physical model is the first step in the device-application connecting process, followed by the electrical model. The hybrid behavioral-analytical power loss model for HF buck converter from [23] can accurately calculate power losses even at low load and high frequency conditions and can be applied here.

The proposed physical model was verified when the results of the Simplorer simulations that used the curves obtained in this work, were compared with the efficiency measurements of the buck converter (Fig. 20). It can be seen that at each switching frequency, good agreement between the measured values and simulation was obtained, especially at 20MHz in the low power range, which is the area of interest in our application.

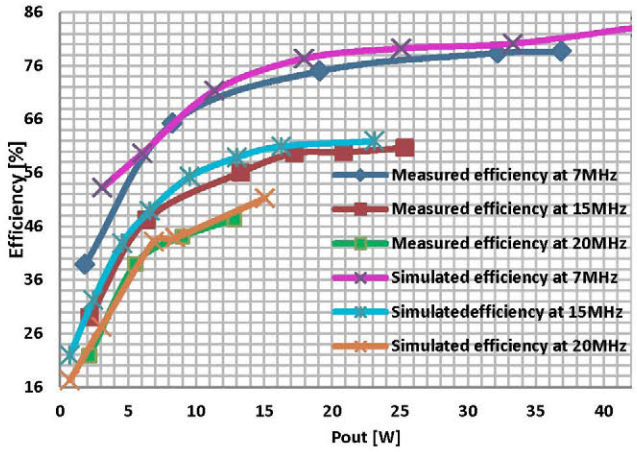

Figure 20. Measured and simulated efficiency curves for HF buck converter

VI. CONCLUSIONS AND FUTURE WORK

Fully analytical physical model of a GaN High Electron Mobility Transistor with the field plate structure has been presented in the paper. Modeled output characteristics I_d (V_{ds}, V_{gs}) of the device showed good correspondence with measured curves, especially in the linear region which is the area of interest in our application. On the other hand, model for input, output and reverse capacitance dependence on V_{ds} in the subthreshold regime, was obtained and experimentally confirmed. The model was verified through the comparison of simulation and experimental efficiency values of the high frequency buck converter. Good agreement was obtained, especially at low output power and high switching frequency which is the area of interest for transmission of wide bandwidth high Peak-to-Average Power Ratio signals.

In order to perform more accurate analysis, it is necessary to obtain total losses breakdown of the HF buck converter. Using the presented dependencies of the device capacitances and on-resistance on the design parameters, it will be possible to optimize the geometry of the device (in terms of width and length of electrodes and field plate), aluminum mole fraction in AlGaN layer and number of paralleled fingers [24] for our application.

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REFERENCES

[1] M. Rodriquez, Y. Zhang, D. Maksimovic, "High-frequency PWM Buck Converters Using GaN-on-SiC HEMTs" *IEEE Trans. on Power Electronics*, vol. 29, no. 5, pp. 2462-2473, May 2014

[2] http://epc-co.com/epc

[3] http://www.infineon.com/

[4] K S. Karmaklar, M. S. Shur, G. Simin, M. A. Khan , "Field-plate Engineering for HFETs," *IEEE Trans. on Electron Devices*, vol. 52, no. 12, pp. 2534-2540, December 2005

[5] H. Huang, Y. C. Liang, G. S. Samudra, T. Chang, C. Huang, "Effects of Gate Field Plates on the Surface State Related Current Collapse in AlGaN/GaN HEMTs" *IEEE Trans. on Power Electronics*, vol. 29, no. 5, pp. 2164-2173, May 2014

[6] M. Meneghini, D. Bisi, D. Marcon, M. Van Hove, T. Wu, S. Decoutere, G. Meneghesso, E. Zanoni, "Trapping and Reliability Assessment in D-Mode GaN-Based Mid-HEMTs for Power Applications", *IEEE Trans. on Power Electronics*, vol. 29, no. 5, pp. 2199-2207, May 2014

[7] J. Hoversten, *Efficient and linear transmitters for high peak-to-average ratio signals*, Ph.D. Thesis, Dept. of Electrical and Computer Engineering, University of Colorado, Boulder, 2010

[8] F. Wang, A. Yang, D. Kimball, L. Larson, P. Asbeck, "Design of a Wide-Bandwidth Envelope Tracking Power Amplifiers for OFDM Applications," *IEEE Trans. Microwave Theory and Techniques*, vol. 53, no. 4, pp. 1244-1255, April 2005

[9] C. Yu, A. Zhu, "A Single Envelope Modulator-Based Envelope Tracking Structure for Multiple-Input and Multiple-Output Wireless Transmitters," *IEEE Trans. Microwave Theory and Techniques*, vol. 60, no. 10, pp. 3317-3327, Oct. 2012

[10] F. H. Raab, "Intermodulation Distortion in Kahn- Technique Transmitters," *IEEE Trans. Microwave Theory and Techniques*, vol. 44, no. 12, pp. 2273-2278, Dec. 1996

[11] F. Wang, D. Kimball, J. D. Popp, A. H. Yang, D. Y. Lie, P. Asbeck, L. E. Larson, "An Improved Power-Added Efficiency 19-dBm Hybrid Envelope Elimination and Restoration Power Amplifier for 802.11g WLAN Applications," *IEEE Trans. on Microwave Theory and Techniques*, vol. 54, no. 12, pp. 4086-4099, Dec. 2006

[12] M. Norris, D. Maksimovic, "10 MHz Large Signal Bandwidth, 95% Efficient Power supply for 3G-4G Cell Phone Base Stations," in Proc. *IEEE APEC*, 2012, pp. 7-13

[13] D. Cucak, M. Vasic, O. Garcia, J. Oliver, P. Alou, J. A. Cobos, "Optimum Design of an Envelope Tracking Buck Converter for RFPA using GaN HEMTs", in *Proc. IEEE ECCE*, 2011, pp. 1210-1216

[14] M. K. Chattopadhyay, Device Modeling of AlGaN/GaN High Electron Mobility Transistors (HEMTs)- an Analytical Approach, Saarbrücken, Germany, LAP LAMBERT, 2010

[15] O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, L. F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, J. Hilsenbeck, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaN/GaN heterostructures", *Journal of Applied Physics,* vol. 85, no. 6, pp. 3222-3233, March 1999

[16] S. Khandewal, N. Goyal, T. A. Fjeldly, "A Physics –Based Analytical Model for 2DEG Charge Density in AlGaN/GaN HEMT devices" *IEEE Trans. on Electron Devices*, vol. 58, no. 10, pp 3622-3625, Oct 2011

[17] M. Saleh, M. Nokali, "A DC Model for the HEMT including the effect of parasitic conduction", in Proc. IEEE University/Government/Industry Microelectronics Simposium 1991, pp. 164-168

[18] J.Si, J. Wei, W. Chen, B. Zhang, "Electric Field Distribution Around Drain-Side gate Edge in AlGaN/GaN HEMTs: Analytical Approach", *IEEE Trans. on Electron Devices*, vol. 60, no. 10, pp 3223-3229, Oct 2013

[19] A. Bansal, B. C. Paul, K. Roy, "An analytical Fringe Capacitance Model for Interconnects Using Conformal Mapping ", *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 25, no. 12, pp 2765-2774, Dec 2006

[20] H. Ahn, M. Nokali, "An Analytical Model for High Electron Mobility Transistors", *IEEE Trans. on Electron Devices*, vol. 41, no. 6, pp 874-878, June 1994

[21] X. Cheng, M. Li, Y. Wang, "Physics-Based Compact Model for AlGAN/GaN MODFETS with Close-Formed I-V and C-V Characteristics ", *IEEE Trans. on Electron Devices*, vol. 56, no. 12, pp 2881-2887, Dec 2009

[22] S. Khandelwal, T. A. Fjeldly, "A Physics Based Compact Model for I-V and C-V characteristics in AlGaN/GaN HEMT devices", *Journal. on Solid State Electronics,* vol. 76, pp 60-66, July 2012

[23] D. Diaz, M. Vasic, O. Garcia, J. A. Oliver, P. Alou, J. A. Cobos, "Hybrid behavioral-analytical loss model for a high frequency and low load DC-DC buck converter", in Proc. IEEE Energy Conversion Congress and Exposition 2012 (ECCE), pp. 4288-4294

[24] Reiner, R.; Waltereit, P.; Benkhelifa, F.; Muller, S.; Müller, S.; Walcher, H.; Wagner, S.; Quay, R.; Schlechtweg, M.; Ambacher, O., "Fractal structures for low-resistance large area AlGaN/GaN power transistors," Power Semiconductor Devices and ICs (ISPSD), 2012 24th International Symposium on , vol., no., pp.341,344, 3-7 June 2012